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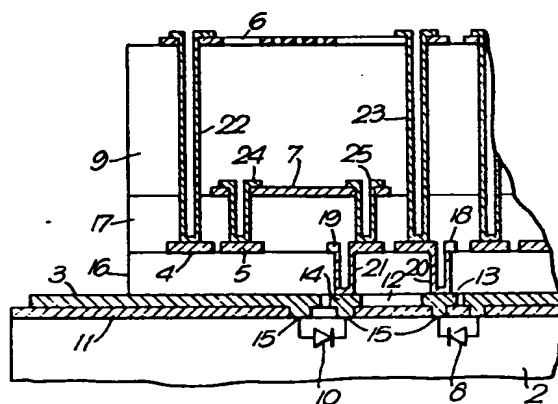
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54 Thermal image generating device.

57 A thermal image producing device comprising an array of separately addressable thin-film resistors (6) on a substrate (2) with a heat sink at its rear face and, so as to render the heat flux flowing through the substrate into the heat sink spatially and temporarily uniform, e.g. to avoid smearing, an array of compensating resistors (7), each beneath a respective one of the image producing resistors and separated therefrom by an insulating layer (9). Each compensating resistor (7) is controlled so that, it and its associated image producing resistor (6) together, produce a uniform total heat flux.



THERMAL IMAGE PRODUCING DEVICE

U.K. Patent Specification No. 2117957 discloses a thermal image generating device for use in developing and testing infra-red radiation sensitive electro-optical equipment, the device comprising a substrate supporting an array of resistor elements which are able to be selectively heated by the passage of electrical current therethrough so as to produce, from the array, a controllable thermal image made up of pixels which correspond to respective ones of the resistor elements.

At the rear of the substrate, a heat sink is provided to receive and dissipate the heat produced by the resistors. A problem with such a device is that, since the temperatures of the elements are not all the same (this must be so as to produce an image), the heat flux flowing into the heat sink is not spatially uniform and, since a fixed image, the heat flux flowing into the heat sink at one point on its surface will also vary with time.

An object of the invention is to provide a thermal image generating device comprising a resistor array from which the produced heat flux is at least more spatially and temporarily uniform.

According to one aspect of the present invention, there is provided a thermal image producing device comprising an array of first and second resistor elements and electrical current supply means connected to the elements for enabling them to be selectively heated by the passage of electrical current therethrough, the elements being arranged such that heat produced by the first elements is receivable from the device as a controllably variable thermal image while the

heat produced by the second elements renders the distribution of the heat flux produced by all the elements substantially uniform over the area of the array.

According to a second aspect of the invention there is provided a thermal image producing device comprising a first planar array of resistor elements, electrical current supply means connected to the elements of the first array for enabling them to be selectively heated by the passage of current therethrough and thereby to produce a controllably variable thermal image at one side of the array, a second planar array of resistor elements positioned at the other side of the first array with each element of the second array adjacent a respective corresponding one of the elements of the first array but insulated from said respective corresponding one element of the first array, and from said one side of the first array, by dielectric material; and cooling means for receiving heat from the said other side of the first array and from said second array, the electrical current supply means being further connected to the elements of the second array for enabling them to be selectively heated by the passage of current therethrough to render the distribution of the heat flux produced by all the elements substantially uniform over the area of the arrays.

For a better understanding of the invention, reference will be made, by way of example, to the accompanying drawings, in which:-

Figure 1 is a perspective view of part of a thermal image producing device,

Figure 2 is a plan view including one pixel resistor of the device,

Figure 3 is a partly diagrammatic sectional view on line 3.3 in figure 2,

Figure 4 is a circuit diagram of part of the figure 1 device and its drive electronics,

Figure 5 is a circuit diagram for illustrating a modification of the figure 1 device.

The device shown in drawing Figure 4 of UK Patent Specification No. 2117959 comprises a two-dimensional planar array of thin-film resistors mounted on respective dielectric portions which are in turn mounted on a substrate with a bus-bar structure arranged between the dielectric portions and the substrate. The bus-bar structure comprises a matrix of column and row bus-bars, each resistor being connected between one row and, via a series diode, one column bus-bar. By applying appropriate currents to the column bus-bars while strobing the row bus-bars, the resistor elements may be selectively heated to produce a controllably variable thermal image. In a modification shown in Figure 7 of the prior specification, the bus-bars are used to address and control the potentials stored on a matrix of capacitors which, in turn, control the currents flowing through respective ones of the resistor elements. The capacitors thus act as latching elements which maintain the temperatures of the resistor elements between successive updates thereof.

In the device to be described herein, for each resistor element which forms part of the image producing array, i.e. for each 'emitter'

resistor, there is provided a second compensating resistor similar (if not identical) to the emitter resistor but positioned on the substrate directly below the emitter resistor and separated from it by a dielectric layer. The resistors are independently addressed so that the total power dissipated is constant: this is controlled by the external drive electronics. To a first order approximation the compensation technique gives the following advantages:

- (i) The total heat flux leaving the rear of the substrate is uniform and constant; i.e. there is no variation over the area of the device or with time.
- (ii) The uniform heat flux means that no lateral temperature gradients will exist even if a large temperature gradient vertically into the heat sink exists. (in the uncompensated case the heat flux was temporally and spatially varying).
- (iii) The spatial uniformity allows a large vertical temperature gradient to exist without thermally smearing the displayed image thus heat sinking across a metal heat sink to a large finned area in say liquid Nitrogen could be used. Instead of the latter form of cooler, one which makes use of nucleate boiling could be used, but this is not preferred because nucleate boiling may impose a peak heat flux thus limiting the maximum display temperature for a given time response.

The image generating device of figures 1 to 4 comprises a deeply finned Molybdenum heatsink 1 supporting a silicon substrate 2. The

substrate supports a structure including a series of parallel row bus-bars 3, a series of parallel column bus-bars 4 and 5 which are orthogonal to the row bus-bars so that the bus-bars form a matrix, and two arrays of thin-film resistors 6 and 7. The resistors 6 are exposed at the outer surface of the structure and are used to produce the thermal image. They are connected to respective ones of the column bus-bars 4 and, via a respective diode 8, to a respective one of the row bus-bars 3. Thus, via the bus-bars 3 and 4, the resistors 6 can be selectively addressed and heated by the passage of electrical current therethrough to produce the required image. Meanwhile, the resistors 7 lie beneath respective ones of the resistors 6, separated therefrom by an insulation layer 9 of Polyimide, and are each connected between that respective column bus-bar 5 which is adjacent to the bus-bar 4 connected to the overlying resistor 6 and, via a diode 10, to the respective bus-bar 3 coupled to that overlying resistor 6. Thus, via the bus-bars 3 and 5, the resistors 7 can also be selectively addressed and supplied with electrical current.

Referring to figures 2 and 3, the substrate 2 is provided with a surface layer 11 of oxide dielectric and the diodes 8 and 10 are integrated into the substrate. The row bus-bars 3 are deposited on layer 11. For each associated pair of the resistors 6 and 7, ie each resistor 6 and the underlying resistor 7, an aperture 12 is provided in the row bus-bar and two connection pads 13 and 14 are provided on layer 11 within the aperture.

The row bus-bars and the pads 13 and 14 are connected to the underlying structures of the diodes 8 and 10 via holes 15 in the oxide

layer 11. The diodes 8 and 10 are illustrated diagrammatically. The choice of physical structure and the means for forming them, and any consequent modification of the row bus-bar and pad geometry, are all design details within the capabilities of those skilled in the art. By way of example, each diode might be fabricated, in an epitaxial n^- layer grown on a p^- substrate, within a reverse-biassed 'bucket diode' formed by an encircling p region and the underlying p^- substrate, the function of the bucket diode being to electrically isolate the diodes 8 and the diodes 10 one from another. Each diode 8 and 10 could have a central anode contact and several cathode contacts around it. Then, of course, the detail geometry of the pads and row bus-bars will need appropriate adaptation from what is shown in figure 3.

First and second relatively thin layers 16 and 17 of polyimide are deposited over the bus-bars 3, pads 13 and 14 and oxide layer 11 and the much thicker polyimide layer 9 is provided over the layers 16 and 17. The column bus-bars 4 and 5 are formed on the first Polyimide layer 16 along with, for each pair of resistors 6 and 7, two connection tags 18 and 19 which connect by way of 'vias' 20 and 21 respectively (through-connections - for example plated-through holes as shown) to respective ones of the pads 13 and 14. The resistors 6 and 7, formed by etching of respective layers of titanium, are provided on the outer surfaces of respective ones of the Polyimide layers 9 and 17. They are connected, one side of each to a respective one of the corresponding pair of adjacent column bus-bars 4 and 5 and the other side of each to a respective one of the corresponding two tags 18 and 19, by way of vias 22, 23, 24 and 25. The holes for the vias 20 to 25 could be formed by plasma etching.

As shown in figure 4, the row bus-bars 3 are connected by way of respective amplifiers 26 to respective ones of a series of row selection output terminals 27 of a control circuit 28 which has two further output terminals 29 and 30 connected to respective ones of a gating arrangement 31 and a buffer store 32. Image signals, say from an image frame store fed by a t.v. camera (not shown) viewing a scene to be reproduced as an image or from an image generating computer (not shown), are received by gating arrangement 31 and, on command from control circuit 28, are passed onto the buffer store 32 to update its content. The function of the buffer store is to allow for the likelihood that the frame update rate of the image signal providing apparatus, ie the t.v. camera or computer say, will be much slower than the best update rate for the thermal image producing device. Thus, the buffer store content may be updated via the gating arrangement 31 at the frame rate of the signal providing apparatus, say every 25 milliseconds, and then read out from the buffer store 32 to control the image generator many times within each 25 millisecond period. Under the control of circuit 28, the content of store 32 is read, row-by-row, into a register 33. Each digital pixel signal of the row held in the register 33 is fed to a respective one of a plurality of devices 34, one for each of the column bus-bars 4 and 5, which produce respective resistor drive currents corresponding to the digital pixel signals. The drive currents are fed via amplifiers 35 to the column bus-bars 4 and 5. Meanwhile, the circuit 28 applies a potential, via the appropriate one of its terminal 27 and the associated amplifier 26, only to the row bus-bar 3 which corresponds to

the image pixel row held in the register 33 so as to turn on the diodes 8 and 10 connected to that row bus-bar. The potential on the other row bus-bars at this time is made such as to keep the diodes connected thereto turned off. Thus, the resistors 6 and 7 of the corresponding image generating array row pass the respective drive currents, ie this row is updated. After any row has been so updated, the next image signal row is read into the register 33 and the corresponding next row bus-bar has the diode turn on potential applied thereto. When all the rows have been updated, the sequence is repeated. As noted, the sequence of updating the generated thermal image may occur many times for each update of the image frame held in the buffer store 32.

Compensation can be applied to latching circuits as shown in Figure 5 which therefore has the combined advantages of the two ideas. Each pixel circuit connects to a corresponding row bus-bar 50 and two column bus-bars 51 and 52 as before, but now also receives drive power from drive rails 53 and 54. The emitter resistor 6~~5~~ is connected between rail 53 and the collector of transistor 56 of which the base is connected to be controlled by the potential stored on capacitor 57. That potential is in turn updated, each time the row bus-bar is strobed, by the signal applied via transistor 58 from column bus-bar 51. A similar circuit controls the current flowing through the compensating resistor 7.

Even if the resistors 6 and 7 in the described embodiments always dissipate the same total power there can still be transient imbalances. For example suppose that at $t = 0$, the power in resistor

6 is zero (hence resistor 7 dissipates P_{\max}) and then a step function change reverses this $R_6 \Rightarrow P_{\max}$ $R_7 \Rightarrow 0$; the time constant for heat to reach the substrate from R_6 is longer than from R_7 ; the effect of R_7 changes therefore is seen by the substrate before the increase in flux from R_6 ; thus at the changeover there will be a transient drop in the flux in the substrate.

In order to reduce the thermal transient; the signal to R_7 can be delayed by a time equivalent to the response of R_6 . A simple first order electronic filter incorporated at each pixel would suffice to do this. It may also be possible to incorporate this response shaping in the signal handling external to the device.

A further advantage of the uses of the compensating resistors is that running at constant power eases the design of the drive electronics: with the prior art device to drive the device it may be necessary to have the electronics dump the compensating power into dummy loads.

CLAIMS

1. A thermal image producing device comprising an array of first and second resistor elements and electrical current supply means connected to the elements for enabling them to be selectively heated by the passage of electrical current therethrough, the elements being arranged such that heat produced by the first elements is receivable from the device as a controllably variable thermal image while the heat produced by the second elements renders the distribution of the heat flux produced by all the elements substantially uniform over the area of the array.

2. A thermal image producing device comprising a first planar array of resistor elements, electrical current supply means connected to the elements of the first array for enabling them to be selectively heated by the passage of current therethrough and thereby to produce a controllably variable thermal image at one side of the array, a second planar array of resistor elements positioned at the other side of the first array with each element of the second array adjacent a respective corresponding one of the elements of the first array but insulated from said respective corresponding one element of the first array, and from said one side of the first array, by dielectric material; and cooling means for receiving heat from the said other side of the first array and from said second array, the electrical current supply means being further connected to the elements of the

second array for enabling them to be selectively heated by the passage of current therethrough to render the distribution of the heat flux produced by all the elements substantially uniform over the area of the arrays.

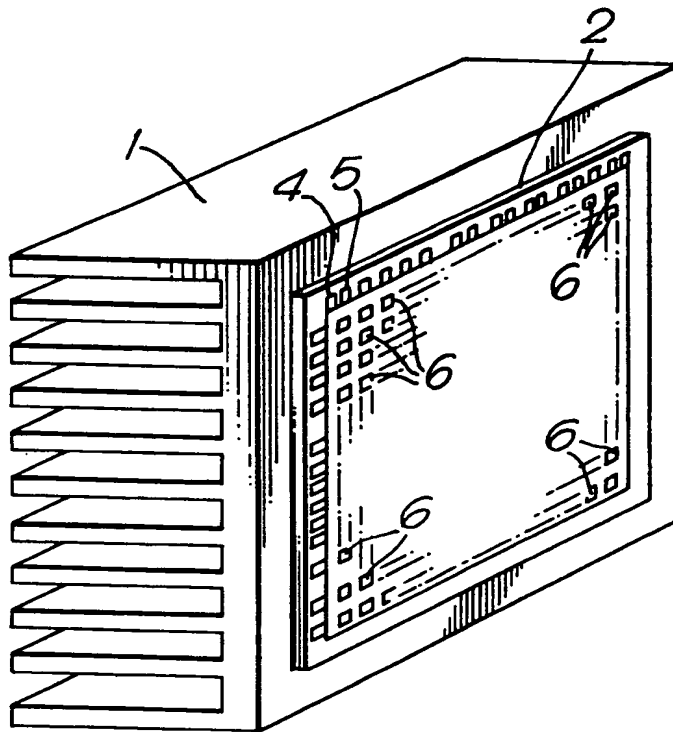
Fig. 1.

Fig. 2.

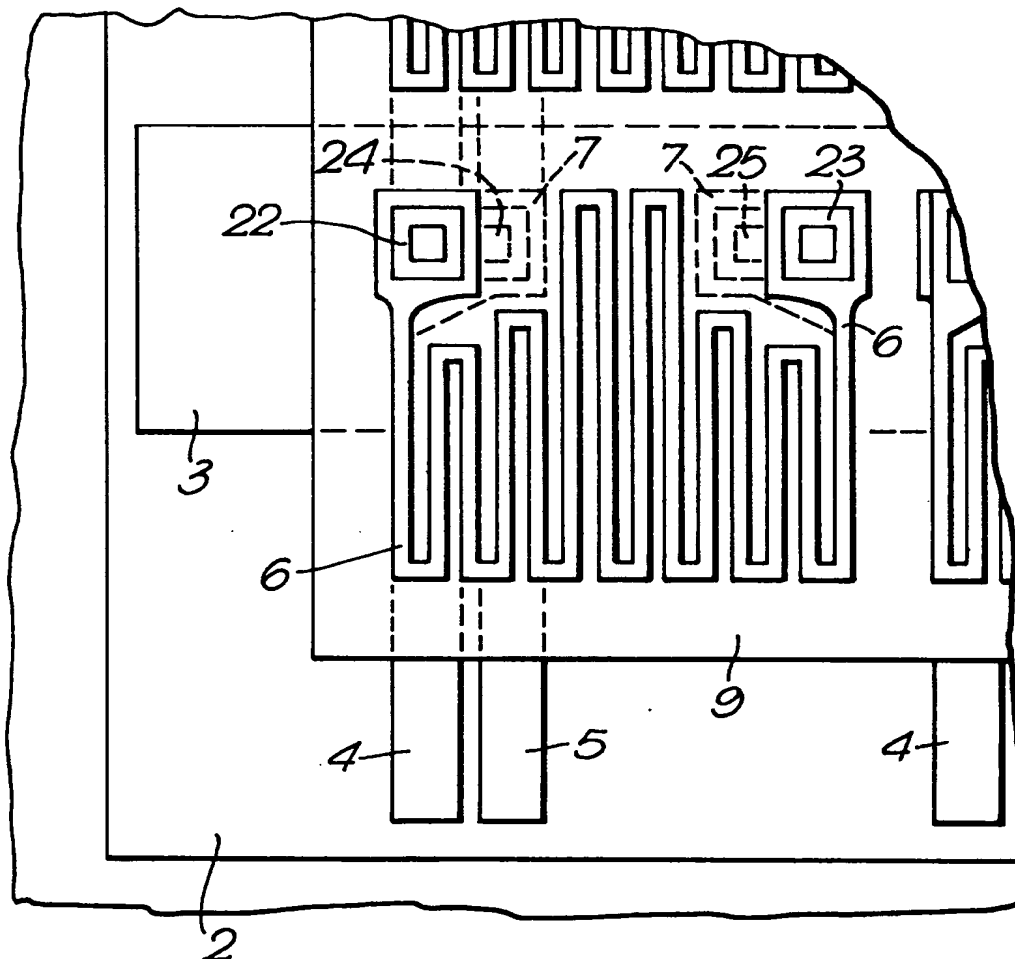
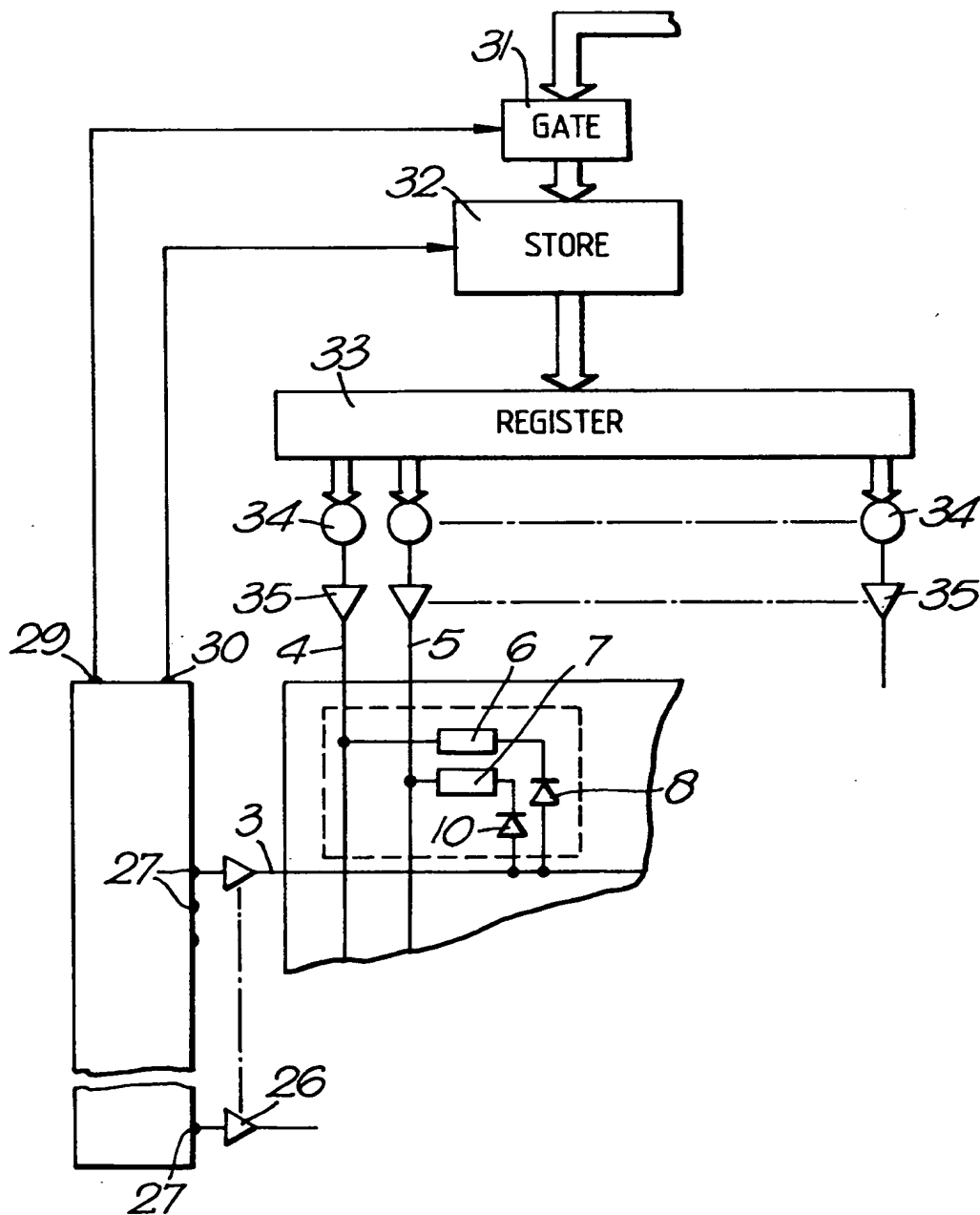


Fig. 3.

This diagram shows a cross-section of a device with multiple vertical chambers. At the base, there is a horizontal layer 11. Below this, a series of valves 15 are shown, with arrows indicating flow direction. The valves are connected to a lower chamber 2. Above the valves, there are several horizontal layers: 16, 17, and 18. The main body of the device consists of vertical walls 9 and 23. Inside, there are horizontal structures 7 and 24. Other labeled parts include 3, 4, 5, 6, 8, 10, 12, 13, 14, 19, 20, 21, 22, and 25. The diagram illustrates the internal components and flow paths of the device.

The circuit diagram shows a differential amplifier with two input transistors, 58 and 56, whose sources are connected to a common source node 54. Each input transistor has a current mirror load consisting of two diode-connected transistors and a tail resistor (57). The outputs of the differential pair are taken from the drains of transistors 58 and 56, which are connected to a differential-to-single-ended converter. This converter consists of two parallel branches, each containing a resistor (6) in series with a diode-connected transistor. The outputs of this converter are connected to the signal lines 51 and 52.

Fig. 4.





European Patent
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EUROPEAN SEARCH REPORT

0218372

Application number

EP 86 30 6856

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|-----------------------------------------------|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
| A, D | GB-A-2 117 957 (BRITISH AEROSPACE PLC) * Page 1, column 1, lines 16-25; page 1, column 2, line 127 - page 2, column 1, line 8; page 2, column 1, line 53 - page 2, column 2, line 64; figure 4 * | 1 | G 01 R 31/28 B 41 J 3/20. F 41 J 9/13 |
| A | --- US-A-4 090 060 (JORNOD) * Column 2, line 23 - column 4, line 26; figures 1,3,4 * | 1 | |
| A | --- EP-A-0 044 756 (THOMSON-CSF) * Page 3, line 5 - page 8, line 2; figures 1-3,5 * | 1 | |
| A | --- US-A-4 386 360 (MURAYAMA) * Column 1, line 1 - column 2, line 24; figures 1,2 * | 2 | TECHNICAL FIELDS SEARCHED (Int. Cl.4) |
| A | --- PATENTS ABSTRACTS OF JAPAN, vol. 5, no. 43 (M-60)[715], 23rd March 1981; & JP-A-56 178 (HITACHI SEISAKUSHO K.K.) 06-01-1981 ----- | 2 | G 01 R 31/00 B 41 J 3/00 F 41 J 9/00 |
| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 12-12-1986 | Examiner TRELEVEN C. |
| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : member of the same patent family, corresponding document</p> | | | |